
CH7117B HDMI to SDTV/HDTV/BT656/VGA Converter with Flexible Scaler

FEATURES

- Multiple input formats supported:
 - HDMI Receiver compliant with HDMI 1.4 specification and DVI 1.0 specification. Support input resolution up to 1080p. Support Hot Plug detection for HDMI/DVI
 - Single channel 18-bit/24-bit LVDS receiver support display resolution up to 1366x768
 - ITU-R 601 or ITU-R 656 compatible YCbCr 4:2:2 input format with embedded syncs. Support resolution up to 1280 x 720@60Hz for YCbCr 4:2:2 input
- Support multiple output formats:
 - SDTV format (CVBS or S-Video output, NTSC and PAL)
 - HDTV format (YPbPr output) for 480p, 576p, 720p, 1080i and 1080P
 - Single channel 18-bit/24-bit LVDS transmitter support display resolution up to 1366x768
 - Analog RGB output for VGA with Triple 9-bit DAC up to 200MHz pixel rate. Sync signals can be provided in separated or composite manner. Support VESA and CEA timing standards up to UXGA and 1920x1080@60Hz
 - ITU-R 601 or ITU-R 656 compatible YCbCr 4:2:2 output format with embedded syncs or separate syncs. Support resolution up to 1280 x 720@60Hz for YCbCr 4:2:2 output
- On-chip Audio encoder which support 8 channel IIS/ S/PDIF audio output
- Flexible scaler engine embedded
- VGA output is compliant with VESA VSIS v1r2 specification
- MCU embedded to handle the control logic
- Support device boot up by automatically loading firmware from EEPROM
- Integrated EDID Buffer
- OSD controller support
- TV connection detection supported
- HDMI input detection supported
- Support Auto Power Saving mode and low stand-by current
- Support 422 to 444 conversion
- Support RGB to YCC conversion in ITU-R BT.601 and 709 color space for SDTV/HDTV/BT656 output
- IIC slave interface is available for debug and

GENERAL DESCRIPTION

Chrontel's CH7117B is an innovative semiconductor device that consists of HDMI receiver, single channel LVDS receiver/transmitter, three separate 9-bit video Digital-to-Analog Converters (DACs), SDTV encoder, HDTV encoder, YCbCr 4:2:2 decoder/encoder and audio encoder, which can convert HDMI / LVDS / BT656 signals into CVBS / S-Video / YPbPr / LVDS / BT656 / Analog RGB outputs with IIS or SPDIF audio output.

The HDMI receiver integrated is compliant with HDMI 1.4b. The DACs are based on current source architecture. The single channel LVDS receiver/transmitter complies with the SPWG or OpenLDI specification, popular LVDS standards used by panel manufacturers. Each input/output LVDS interface is equipped with 4/1 pairs of differential signal buses to support video data and clock. The device's LVDS receiver/transmitter can accept/output maximum video clock frequency for up to 85MHz or 1366x768 resolution in 24-bit color per pixel.

With a powerful scaling engine working together with other video processing circuits, CH7117B will convert the captured input signal with resolution up to 1920x1080@60Hz, which is stored in the internal DDR RAM, into analog video format or LVDS/BT656 signal with any specified resolution.

With sophisticated MCU Embedded, CH7117B support auto-boot and EDID buffer. Leveraging Firmware auto loaded from the External EEPROM, CH7117B can support HDMI input detection, DAC connection detection and can be programmed to enter into Power Saving mode automatically.

The CH7117B also supports up to 8-channel audio input from HDMI port and output from the special audio output port with sample rate up to 192 KHz. Available audio bandwidth depends on the pixel clock frequency, the video format timing, and whether or not content protection re-synchronization is needed.

firmware update.

- Low power architecture
- RoHS compliant and Halogen free package
- Offered in 88 pin QFN package

APPLICATIONS

- Car Infotainment Device
- Converter Box
- Tablet Device
- OTT/IPTV Box

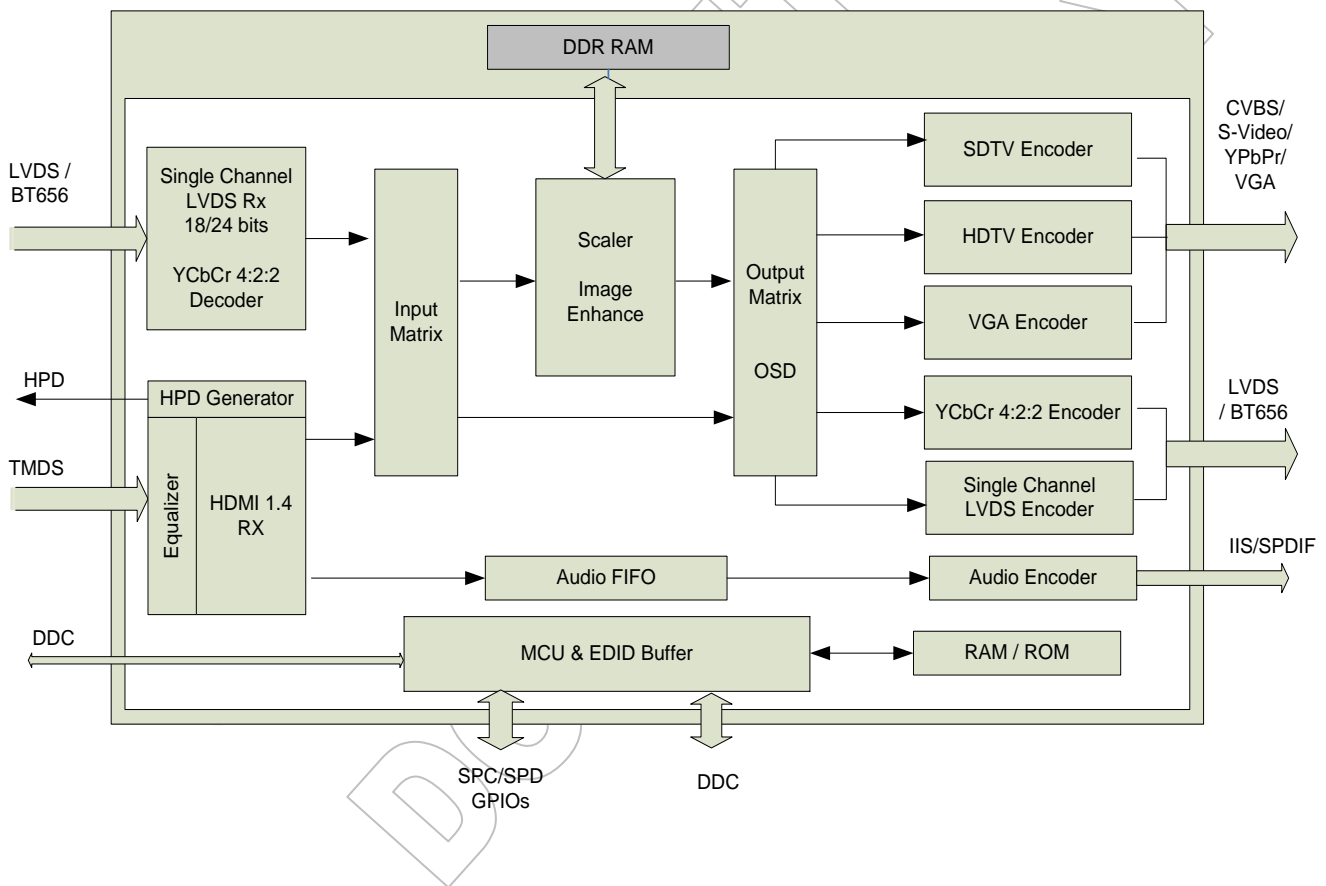


Figure 1: CH7117B Functional Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

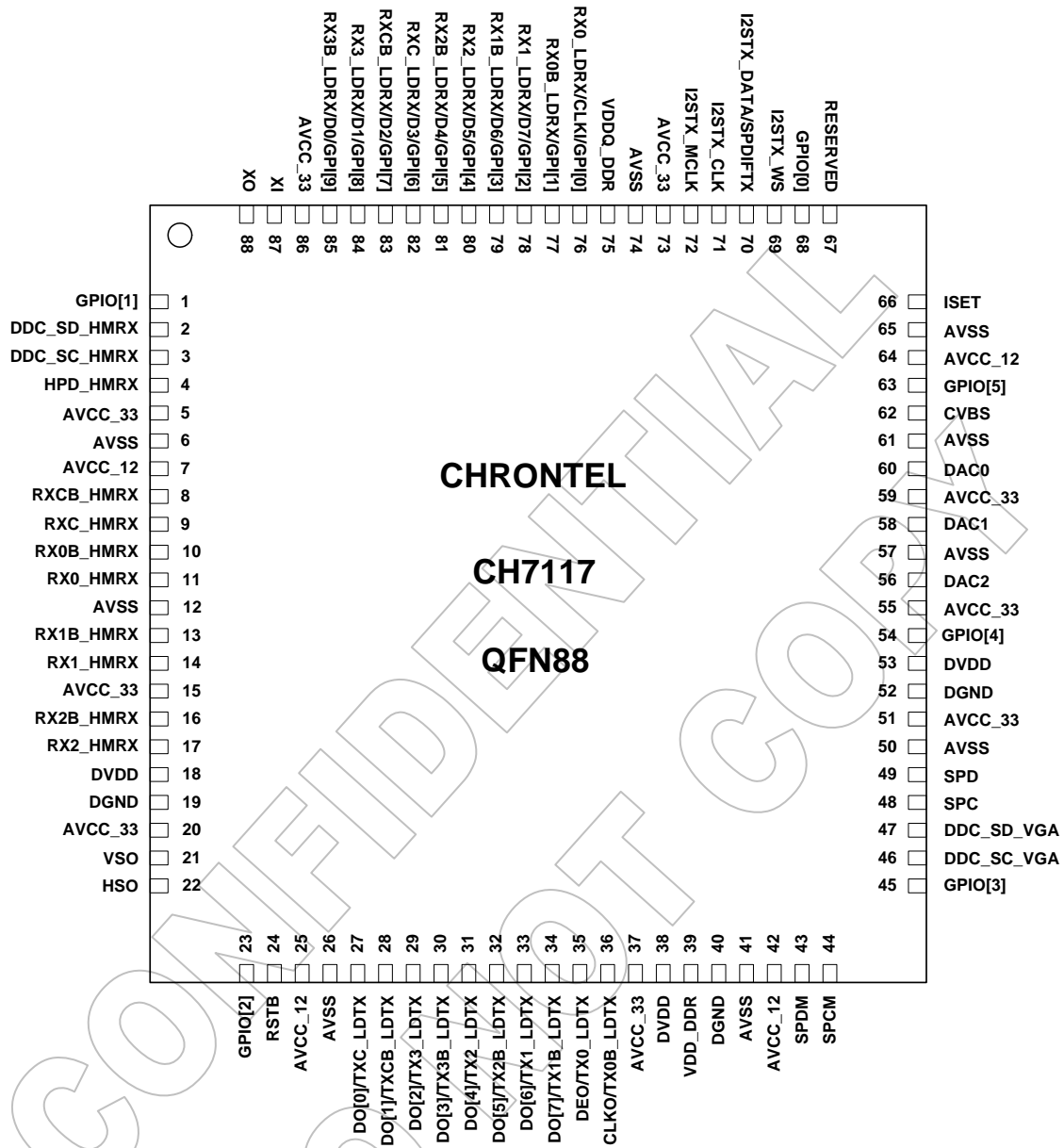


Figure 2: CH7117B 88-pin QFN Pin Out

1.2 Pin Description

Table 1: Pin Name Descriptions

Pin #	Type	Symbol	Description
1,23,45, 54,63,68	In/Out	GPIO[5:0]	General Purpose Input/Output GPIO[0], GPIO[5:4] and I2STX_DATA can be composed for the 8 channel I2S audio data output.
2	In/Out	DDC_SD_HMRX	HDMI Receiver DDC Data Channel This pin functions as the bi-directional data pin of the serial port to HDMI DDC source. This pin will require a pull-up 47 kΩ Resistor to the desired voltage level.
3	In	DDC_SC_HMRX	HDMI Receiver DDC Clock Channel This pin functions as the clock bus of the serial port to HDMI DDC source. This pin will require a pull-up 47 kΩ Resistor to the desired voltage level.
4	Out	HPD_HMRX	HDMI Receiver HPD Output
8	In	RXCB_HMRX	HDMI Rx Negative Clock Channel
9	In	RXC_HMRX	HDMI Rx Positive Clock Channel
10	In	RX0B_HMRX	HDMI Rx Negative Data Channel 0
11	In	RX0_HMRX	HDMI Rx Positive Data Channel 0
13	In	RX1B_HMRX	HDMI Rx Negative Data Channel 1
14	In	RX1_HMRX	HDMI Rx Positive Data Channel 1
16	In	RX2B_HMRX	HDMI Rx Negative Data Channel 2
17	In	RX2_HMRX	HDMI Rx Positive Data Channel 2
21	Out	VSO	VGA/BT656 VSYNC Output Pin
22	Out	HSO	VGA/BT656 HSYNC Output Pin
24	In	RSTB	Chip Reset Low to 0V for reset. Typical High level is 3.3V
27~34	Out	DO[7:0]	BT656 Output Data Pins
35	Out	DEO	BT656 Data Enable Output Pin
36	Out	CLKO	BT656 Output Clock Pin
43	In/Out	SPDM	I2C Master Serial Port Data This pin functions as the bi-directional data pin of the serial port to chip firmware and external EEPROM. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. A pull-low resistor 10 kΩ to ground if unused.
44	Out	SPCM	I2C Master Serial Port Clock This pin functions as the clock bus of the serial port to chip firmware and external EEPROM. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. A pull-low resistor 10 kΩ to ground if unused.
46	Out	DDC_SC_VGA	VGA DDC Clock Channel This pin functions as the clock output pin of the serial port to VGA DDC receiver. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level.
47	In/Out	DDC_SD_VGA	VGA DDC Data Channel This pin functions as the bi-directional data pin of the serial port to VGA DDC receiver. This pin will require a pull-up 5.6 kΩ Resistor to

			the desired voltage level.
48	In	SPC	I2C Slave Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up 6.8 kΩ Resistor is required.
49	In/Out	SPD	I2C Slave Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 kΩ Resistor is required.
56	Out	DAC2	HDTV Pb Component / SDTV C Component / Analog B component output
58	Out	DAC1	HDTV Pr Component / SDTV Y Component / Analog G component output
60	Out	DAC0	HDTV Y Component / CVBS / Analog R component output
62	Out	CVBS	CVBS Output Pin Signal switched from DAC0 internally. While this pin is CVBS output enabled, no signal output from the pin of DAC0.
66	In	ISET	Basic Current Set This pin sets the basic current. A 1 kΩ, 1% tolerance resistor should be connected between this pin and ground using short and wide traces.
69	Out	I2STX_WS	I2S Output Channel Select CMOS level signal, typical 3.3 for high, 0 for low.
70	Out	I2STX_DATA	I2S Data Output CMOS level signal, typical 3.3 for high, 0 for low. GPIO[0]&GPIO[5:4] can be configured as I2S data output channels to support up to 7.1 audio output port.
	Out	SPDIFTX	SPDIF Output Channel
71	Out	I2STX_CLK	I2S Output Clock CMOS level signal, typical 3.3 for high, 0 for low.
72	Out	I2STX_MCLK	I2S Output Clock I2S_MCLKO can be configured to be 128/256/384*I2S_CKO through SPP registers CMOS level signal, typical 3.3 for high, 0 for low.
76~85	In	GPI[9:0]	General Purpose Input Pins
87	In	XI	Crystal Input / External Reference Input A parallel resonance crystal should be attached between this pin and XO. An external 3.3V CMOS compatible clock can drive the XI Input.
88	In	XO	Crystal Output A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open.
5,15,20,37,51,55,59,73,86	Power	AVCC_33	Analog 3.3V Power Supply
6,12,26,41,50,57,61,65,74, Thermal Pad	Power	AVSS	Analog Ground
7,25,42,64	Power	AVCC_12	Analog 1.2V Power Supply
18,38,53	Power	DVDD	Digital 1.2V Power Supply

19,40,52	Power	DGND	Digital Ground
39	Power	VDD_DDR	Digital 1.8V Power Supply
75	Power	VDDQ_DDR	Digital 1.8V Power Supply

CONFIDENTIAL
DO NOT COPY

2.0 PACKAGE DIMENSION

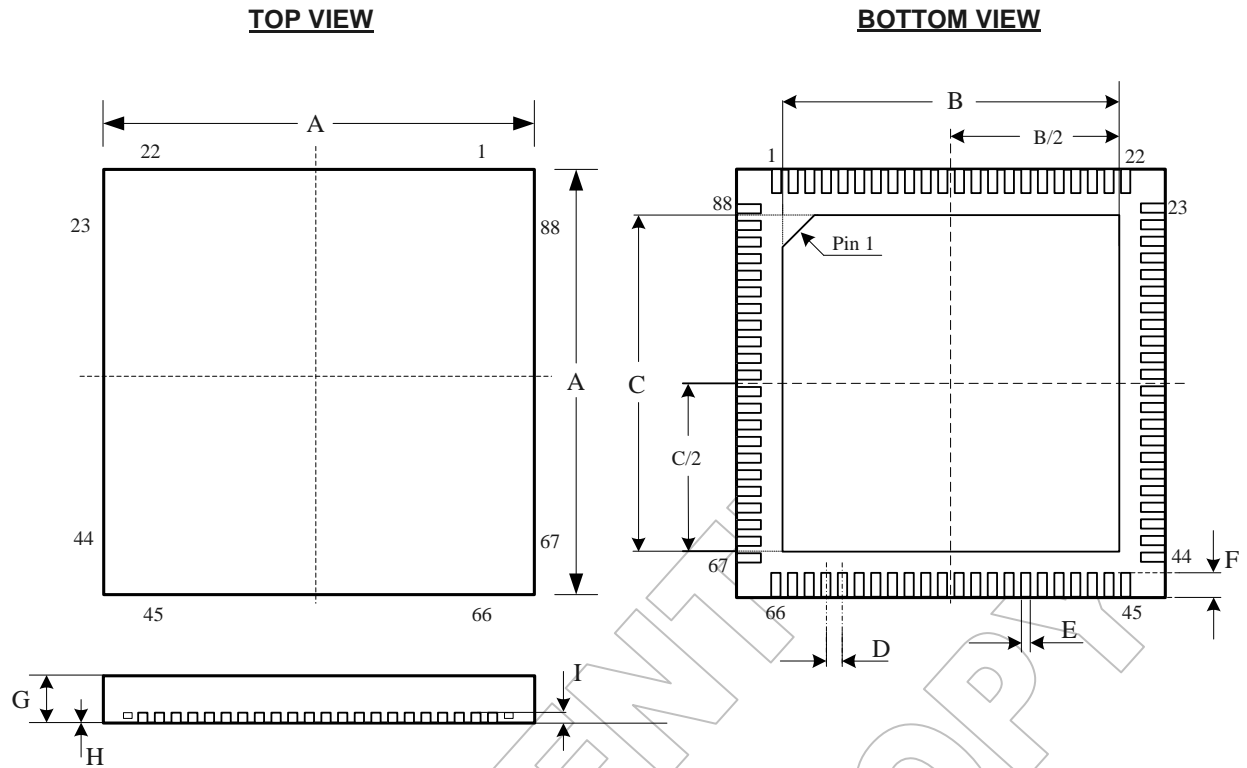


Figure 3: 88 Pin QFN Package (10 x 10 mm)

Table of Dimensions

No. of Leads		SYMBOL								
88 (10 X 10 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	9.90	6.65	6.65	0.30	0.15	0.40	0.80	0	0.20
	NOM	10.00	6.75	6.75	0.40	0.20	0.50	0.85	-	
	MAX	10.10	6.85	6.85	0.50	0.25	0.60	0.90	0.05	

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

Disclaimer

This document provides technical information for the user. Chrontel reserves the right to make changes at any time without notice to improve and supply the best possible product and is not responsible and does not assume any liability for misapplication or use outside the limits specified in this document. CHRONTEL warrants each part to be free from defects in material and workmanship for a period of one (1) year from date of shipment. Chrontel assumes no liability for errors contained within this document. The customer should make sure that they have the most recent data sheet version. Customers should take appropriate action to ensure their use of the products does not infringe upon any patents. Chrontel, Inc. respects valid patent rights of third parties and does not infringe upon or assist others to infringe upon such rights.

Chrontel PRODUCTS ARE NOT AUTHORIZED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS OR NUCLEAR FACILITY APPLICATIONS WITHOUT THE SPECIFIC WRITTEN CONSENT OF Chrontel. Life support systems are those intended to support or sustain life and whose failure to perform when used as directed can reasonably expect to result in personal injury or death.

ORDERING INFORMATION			
Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7117B-BF	88 QFN, Lead-free	Commercial : 0 to 70°C	168/Tray

Chrontel

www.chrontel.com

E-mail: sales@chrontel.com